IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

AMITABH JAIN ET AL.

Serial No. 10/816,776 (TI-34913AA)

Filed April 2, 2004

For: ULTRA SHALLOW JUNCTION FORMATION

Art Unit 2813

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8-14-07

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SUPPLEMENT TO BRIEF ON APPEAL

In response to the Office action dated August 10, 2007, the following is added to replace the SUMMARY OF CLAIMED SUBJECT MATTER originally filed and as a supplement to the Brief on Appeal filed 13 April 2006:

SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to a method for forming ultra shallow junctions in a semiconductor substrate. In order to form ultra shallow junctions, it is essential to retain implanted dopant close to the surface of the device with high active dopant concentrations after the annealing procedure. Prior art annealing procedures have resulted in greater dopant migration away from the device surface than is provided by the present invention, thereby

resulting in increased short channel effects as compared with the procedure of the present invention.

In accordance with the method of the present invention as set forth in claim 1, a dopant species is implanted into the semiconductor substrate with the implanted region being annealed with an ultra high temperature from1050° to 1350° for from about 0.5 to about 3 milliseconds (page 4, lines 3 to 9 and page 8, lines 9 to 12).

In accordance with the invention as set forth in claim 5, a patterned photoresist layer is formed on the semiconductor (Fig 2a, page 6, lines 8-9) and a dopant species is implanted therein (page 6, lines 17 to page 7, line 2). The photoresist layer is removed and the implanted semiconductor is annealed (page 7, line 16 to 19) with a solid phase epitaxy anneal (page 7, lines 19-20) and annealed with a ultra high temperature anneal at temperatures from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds (page 8, lines 9 to 12 and claim 5 as filed)

In accordance with the invention as set forth in claim 9, as shown in Fig. 3, a gate dielectric layer is formed on the semiconductor (page 9, lines 2-3) and a dopant species is implanted adjacent the gate electrode (page 9, lines 10 to 13). The implanted semiconductor is annealed with a solid state epitaxy anneal at a temperature between 550°C and 950°C (page 9, line 22 to page 10, line 2) and annealed with a ultra high temperature anneal from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds (page 10, lines 4 to 7).

In accordance with the invention as set forth in claim 13, as shown in Fig. 3, the is provide a method of forming a gate dielectric layer on the semiconductor (page 9, lines 2-3) and implanting a dopant species adjacent the gate electrode (page 9, lines 10 to 13). Sidewall structures are formed adjacent to the gate electrode (page 10, lines 8 to 10). The

implanted semiconductor is annealed with a solid state epitaxy anneal at a temperature between 550°C and 950°C (page 9, line 22 to page 10, line 2) and annealed with a ultra high temperature anneal from 1100°C to 1350°C for from about 0.5 to about 3 milliseconds (page 10, lines 4 to 7).

Respectfully submitted,

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